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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/663,485	09/15/2003	Takashi Kumamoto	109263-131564	2427
31817	7590	10/05/2005	EXAMINER	
SCHWABE, WILLIAMSON & WYATT PACWEST CENTER, SUITES 1600-1900 1211 S.W. FIFTH AVE. PORTLAND, OR 97204			NADAV, ORI	
			ART UNIT	PAPER NUMBER
			2811	

DATE MAILED: 10/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/663,485

Applicant(s)

KUMAMOTO, TAKASHI

Examiner

Ori Nadav

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 18 July 2005.
2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-5, 7-15 and 17-27 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) 1-5, 7-15 and 17-27 is/are rejected.
7) ☐ Claim(s) _____ is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 7/18/05
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-5, 7-15 and 17-27 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The embodiment of figure 1 describes an intermediate substrate having being located along periphery of the encapsulation material, but not directly coupled to the second non-die side of the second carrier substrate. The embodiment of figure 7 describes an intermediate substrate being directly coupled to the second non-die side of the second carrier substrate, but not being located along periphery of the encapsulation material. There is no support for a device comprising an intermediate substrate being directly coupled to the second non-die side of the second carrier substrate, and being located along periphery of the encapsulation material, as recited in claims 1, 11 and 21.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 21-27 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claimed limitations of placing an intermediate substrate having a plurality of conductive risers disposed therein directly on the first die side of a the first carrier substrate and periphery of the encapsulation material, as recited in claim 21, are unclear as to how the phrase "periphery of the encapsulation material" relates to the claimed structure.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-3, 5, 7-9, 21 and 26, as best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Pu et al. (6,828,665) in view of Juskey et al. (6,507,102) or over Isaak et al. (6,878,571) in view of Pu et al.

Regarding claim 1, Pu et al. teach in figure 3 and related text a microelectronic package array, comprising:

a first microelectronic package 52 including a first carrier substrate 51 having a first die side and a first non-die side, a first die 52 electrically coupled to the first die side, and a land pad 51c on the first die side;

a second microelectronic package 500 comprising a second carrier substrate 54 having a second die side and a second non-die side, a second die electrically coupled to the second die side, and a bond pad 54c on the second non-die side; and

an intermediate substrate 55 (metal pin) having a first side and a second side, the first side being directly coupled to the first die side of the first carrier substrate and the second side being directly coupled to the second non-die side of the second carrier substrate, the intermediate substrate comprising of a substantially solid core having a first side and a second side, the substantially solid core comprising of a material reinforced with a matrix to increase rigidity of the microelectronic package and control the coefficient of thermal expansion of the intermediate substrate.

Pu et al. do not teach a substrate having a solid core comprising a material reinforced with a matrix.

Juskey et al. teach an epoxy resin material reinforced with a matrix (column 3, line 66 - column 4, line 9).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Juskey et al. into the device taught by Isaak et al. in order to provide better mechanical and thermal properties to the device.

Note that a material reinforced with a matrix to increase stiffness and control the coefficient of thermal expansion of the intermediate substrate is a functional language and does not further limit or define the structure and is not given any patentable weight. In any event, prior art's device can be used for the claimed purpose.

Note that the broad recitation of the claim does not provide distinct boundaries between the substrate and the solid core.

Regarding claim 1, Isaak et al. teach in figures 3-4 and related text a microelectronic package array, comprising:

a first microelectronic package 70 including a first carrier substrate 88 having a first die side and a first non-die side, a first die 70 electrically coupled to the first die side, and a land pad 26 on the first die side;

a second microelectronic package 70 comprising a second carrier substrate 88 having a second die side and a second non-die side, a second die 70 electrically coupled to the second die side, and a bond pad 26 on the second non-die side; and

an intermediate substrate 92 having a first side and a second side, the first side being directly coupled to the first die side of the first carrier substrate and the second side being directly coupled to the second non-die side of the second carrier substrate, the intermediate substrate comprising of a substantially solid core having a first side and a second side, the substantially solid core comprising of a material reinforced with a matrix to increase rigidity of the microelectronic package and control the coefficient of thermal expansion of the intermediate substrate.

Isaak et al. do not teach an encapsulation material encasing the first die such that the intermediate substrate is located along periphery thereof.

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Pu et al. teach in figure 3 and related text an encapsulation material 56 (see figure 2e) encasing the first die 52 such that the intermediate substrate 55 (metal pins) is located along periphery thereof.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use an encapsulation material encasing the first die such that the intermediate substrate is located along periphery thereof in Isaak et al.'s device in order to provide better protection to the die.

Note that a material reinforced with a matrix to increase stiffness and control the coefficient of thermal expansion of the intermediate substrate is a functional language and does not further limit or define the structure and is not given any patentable weight. In any event, prior art's device can be used for the claimed purpose.

Regarding claim 2, the combined device shows an adhesive material (Isaak; a portion of the layer [49] and Pu et al. #54b) disposed on the first side (Isaak; top surface of the substrate [34]) and second side (Isaak; bottom surface of the substrate [34]) of the core; and a conductive riser (Isaak; 32 and Pu et al. #55) disposed within the solid core (Isaak; a portion of the intermediate substrate [34]).

Regarding claims 3 and 26, the combined device shows the intermediate substrate (Isaak; 34 and Pu et al. #55) is mechanically bonded to the first die side (Isaak; 16b) of the first carrier substrate (Isaak; 14b) and the second non-die side (Isaak; 18a) of the

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second carrier substrate (Isaak; 14a) by the adhesive material (Isaak; a portion of the layer [49]).

Regarding claims 5 and 7, the combined device shows the material is a C-stage resin (Juskey et al.; column 3, line 66 - column 4, line 9), and a substrate (Juskey et al.; 14) selected from fiberglass. It would have been obvious to one having ordinary skill in the art at the time the invention was made to use a C-stage resin and a fiberglass substrate in prior art's device in order to improve the quality of the device.

Regarding claims 8 and 9, prior art's device shows the conductive riser is electrically coupled to the land pad of the first microelectronic package and the bond pad of the second microelectronic package, wherein the conductive riser includes a first end and a second end having conductive plating disposed thereon, the first and second ends being electrically bonded to the land pad and the bond pad respectively by the conductive plating.

Regarding claim 21, the method steps are necessitated by the device structure, as disclosed by prior art.

Claims 4 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pu et al. and Juskey et al. or over Isaak et al. and Pu et al., as applied to claims 1-3, 21 and 26 above, and further in view of Sylvester (6,014,317).

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Prior art teaches substantially the entire claimed structure, as applied to claims 1-3, 21 and 26 above, except an adhesive material is a B-stage polymer. Sylvester teaches a B-stage adhesive material (column 21, lines 23-28). It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Sylvester into prior art's device in order to improve the molding characteristics of the adhesive material.

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pu et al. and Juskey et al. or over Isaak et al. and Pu et al., as applied to claims 1-2 and 8-9 above, and further in view of Roh (2004/0050586).

Prior art teaches substantially the entire claimed structure, as applied to claims 1-2 and 8-9 above, except tin conductive plating. Roh teaches the conductive plating is tin (paragraph [0033]). It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Roh into prior art's device in order to improve the conductivity of the device.

Claims 11-13, 15 and 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pu et al. and Juskey et al. or over Isaak et al. and Pu et al., as applied to claims 1-3, 5 and 7-9 above, and further in view of Solberg (6,054,337).

Prior art teaches substantially the entire claimed structure, as applied to claims 1-3, 5 and 7-9 above, including a system board, a memory configured to store data, wherein the memory disposed on the system board and a microelectronic package array

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disposed on the system board. Prior art does not teach a memory coupled to the bus. Solberg teaches memory chips, which are connected to the data bus (column 2, lines 55-58). It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Solberg into prior art's device in order to use the device in an application which requires memory capabilities and in order to operate the device in its intended use by providing interconnect between the chip and the external device. The combined device includes a bus disposed on the system board to facilitate data exchange; a memory configured to store data, the memory disposed on the system board and coupled to the bus; and a microelectronic package array disposed on the system board and coupled to the bus.

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pu et al., Solberg and Juskey et al. or over Isaak et al., Solberg and Pu et al., as applied to claims 11-13 above, and further in view of Sylvester (6,014,317).

Prior art teaches substantially the entire claimed structure, as applied to claims 11-13 above, except an adhesive material is a B-stage polymer. Sylvester teaches a B-stage adhesive material (column 21, lines 23-28). It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Sylvester into prior art's device in order to improve the molding characteristics of the adhesive material.

Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pu et al., Solberg and Juskey et al. or over Isaak et al., Solberg and Pu et al., as applied to claims 11-12 and 18-19 above, and further in view of Roh (2004/0050586).

Prior art teaches substantially the entire claimed structure, as applied to claims 11-12 and 18-19 above, except tin conductive plating. Roh teaches the conductive plating is tin (paragraph [0033]). It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Roh into prior art's device in order to improve the conductivity of the device.

Claims 22-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pu et al. and Juskey et al. or over Isaak et al. and Pu et al., as applied to claim 21 above, and further in view of Clarke (5,145,303).

Prior art teaches substantially the entire claimed structure, as applied to claim 21 above, except placing the microelectronic package array in a vacuum chamber; creating a vacuum in the vacuum chamber; applying heat to the microelectronic package array; applying pressure to the microelectronic package array; releasing the pressure; and cooling the microelectronic package array.

Clarke teaches the microelectronic package in processing chamber (column 1, lines 15-19). It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Clarke into prior art's device in order to enhance the performance and to improve reliability of the microelectronic package. The combined device shows placing the microelectronic package array in a vacuum

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chamber; creating a vacuum in the vacuum chamber; applying heat to the microelectronic package array; applying pressure to the microelectronic package array; releasing the pressure; and cooling the microelectronic package array.

Regarding claim 23, the combined device differs from the claimed invention by not showing creating a vacuum comprises establishing a pressure of about less than 10 kilo Pascals. It would have been obvious to one having ordinary skill in the art at the time the invention was made for creating a vacuum comprises establishing a pressure of about less than 10 kilo Pascals in order to enhance the performance and to improve reliability of the microelectronic package. Furthermore, it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claim 24, the combined device differs from the claimed invention by not showing applying heat comprises raising the temperature to about between 150°C and 350°C. It would have been obvious to one having ordinary skill in the art at the time the invention was made for applying heat comprises raising the temperature to about between 150°C and 350°C in order to enhance the performance and to improve reliability of the microelectronic package. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

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Regarding claim 25, the combined device differs from the claimed invention by not showing applying a pressure comprises increasing the pressure to a range between 0.5 mega Pascals and 10 mega Pascals. It would have been obvious to one having ordinary skill in the art at the time the invention was made for applying a pressure comprises increasing the pressure to a range between 0.5 mega Pascals and 10 mega Pascals in order to enhance the performance and to improve reliability of the microelectronic package. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Response to Arguments

Applicant's arguments with respect to claims 1-5, 7-15 and 17-27 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

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A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660. The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Loke can be reached on 571-272-1657. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A handwritten signature in black ink, appearing to read 'Ori Nadav', is positioned above the printed name.

O.N.
9/30/05

ORI NADAV
PRIMARY EXAMINER
TECHNOLOGY CENTER 2800